

(12) UK Patent Application (19) GB (11) 2 223 652 (13) A

(43) Date of A publication 11.04.1990

(21) Application No 8919495.5

(22) Date of filing 29.08.1989

(30) Priority data

(31) 63223005

(32) 08.09.1988

(33) JP

(71) Applicant

Kabushiki Kaisha Toshiba

(Incorporated in Japan)

72 Horikawa-cho, Saiwai-ku, Kawasaki-shi, Japan

(72) Inventor

Shigenori Tokumitsu

(74) Agent and/or Address for Service

Marks & Clerk

57-60 Lincoln's Inn Fields, London, WC2A 3LS,
United Kingdom

(51) INT CL⁴

H04N 7/01

(52) UK CL (Edition J)

H4T TBBN

H4F FD12X FD2B FD22 FD30K FD30T1 FD42V

FGS

(56) Documents cited

None

(58) Field of search

UK CL (Edition J) H4F FCW FEP FEX, H4T TBBN

TBCX TCHX TDAA TDGA

INT CL⁴ H04N

(54) Display control apparatus for image display system

(57) A first section of display control means (6) stores first data adapted to a predetermined display device (9) in a first memory (7). A second section (6) reads the first data out of the first memory (7) on a time division basis in sync with the predetermined timing of display. A third section (6) converts the first data read from the first memory (7) to second data adapted to a display device (10) different from the predetermined display device. A fourth section (6) stores the second data in a second memory (8). A fifth section (6) reads the second data from the second memory (8) in accordance with timing different from the predetermined display timing.

The system is particularly concerned with displaying videotex images comprising a code frame and a pictorial frame on a binary type LCD matrix display 10, as well as on a color CRT 9. The software in ROM (4) is only needed to control CPU(3) to convert the image data for display on the C.R.T. The conversion of the data in the first memory (7) for storage in the second memory (8) and display on the LCD display is carried out by hardware in the display control (6).

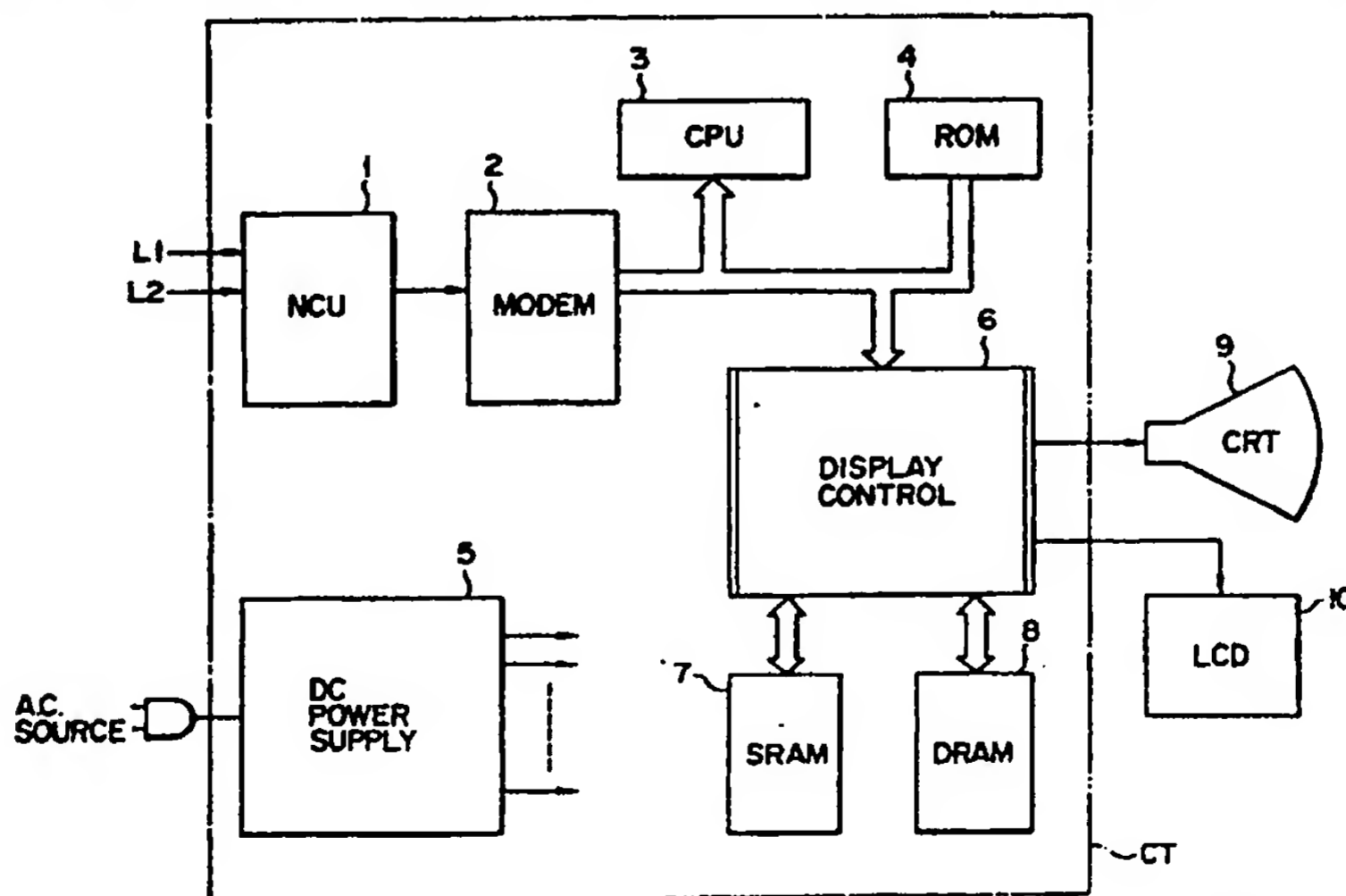


FIG. 1

GB 2 223 652 A

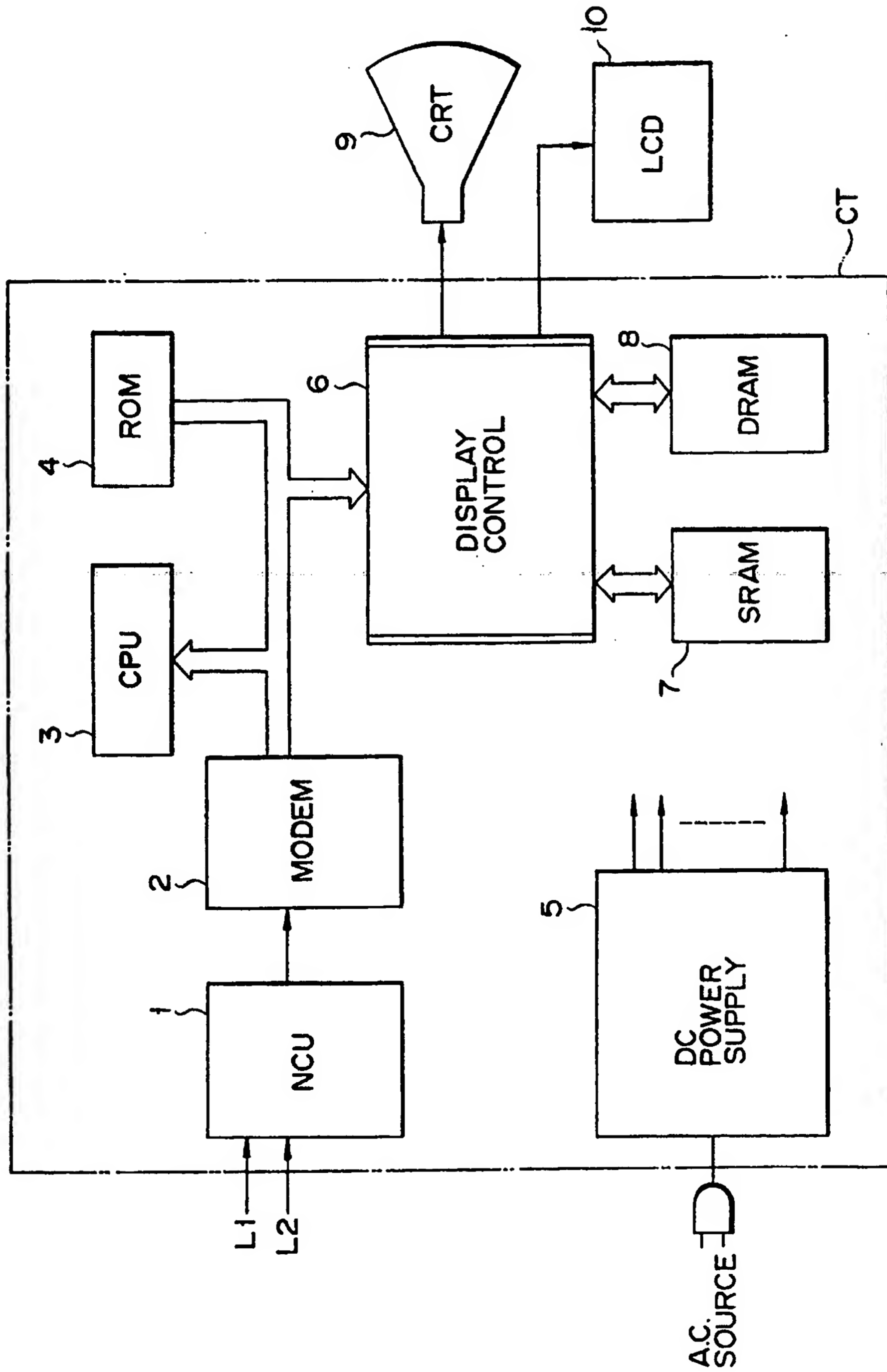
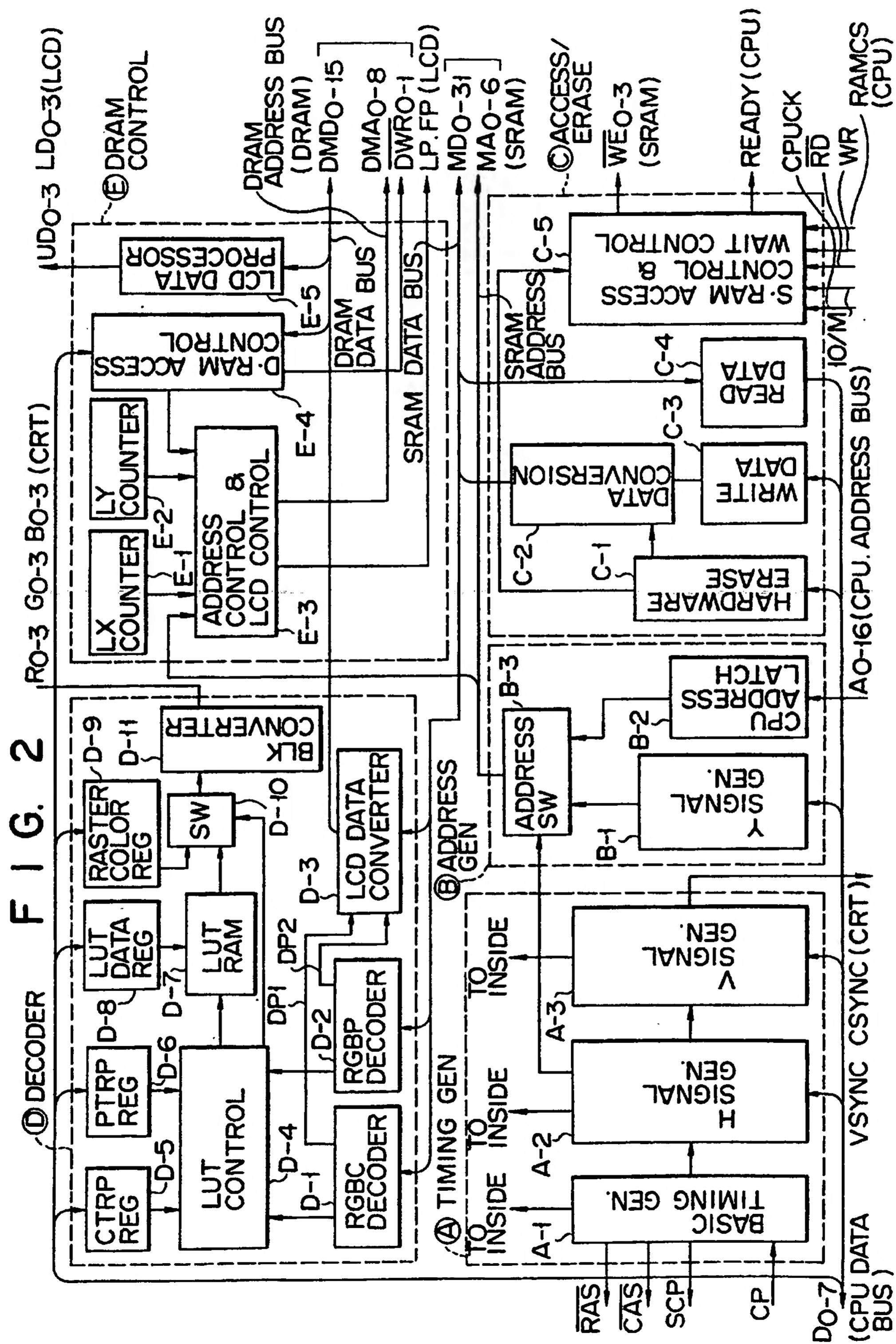


FIG. 1



2223652

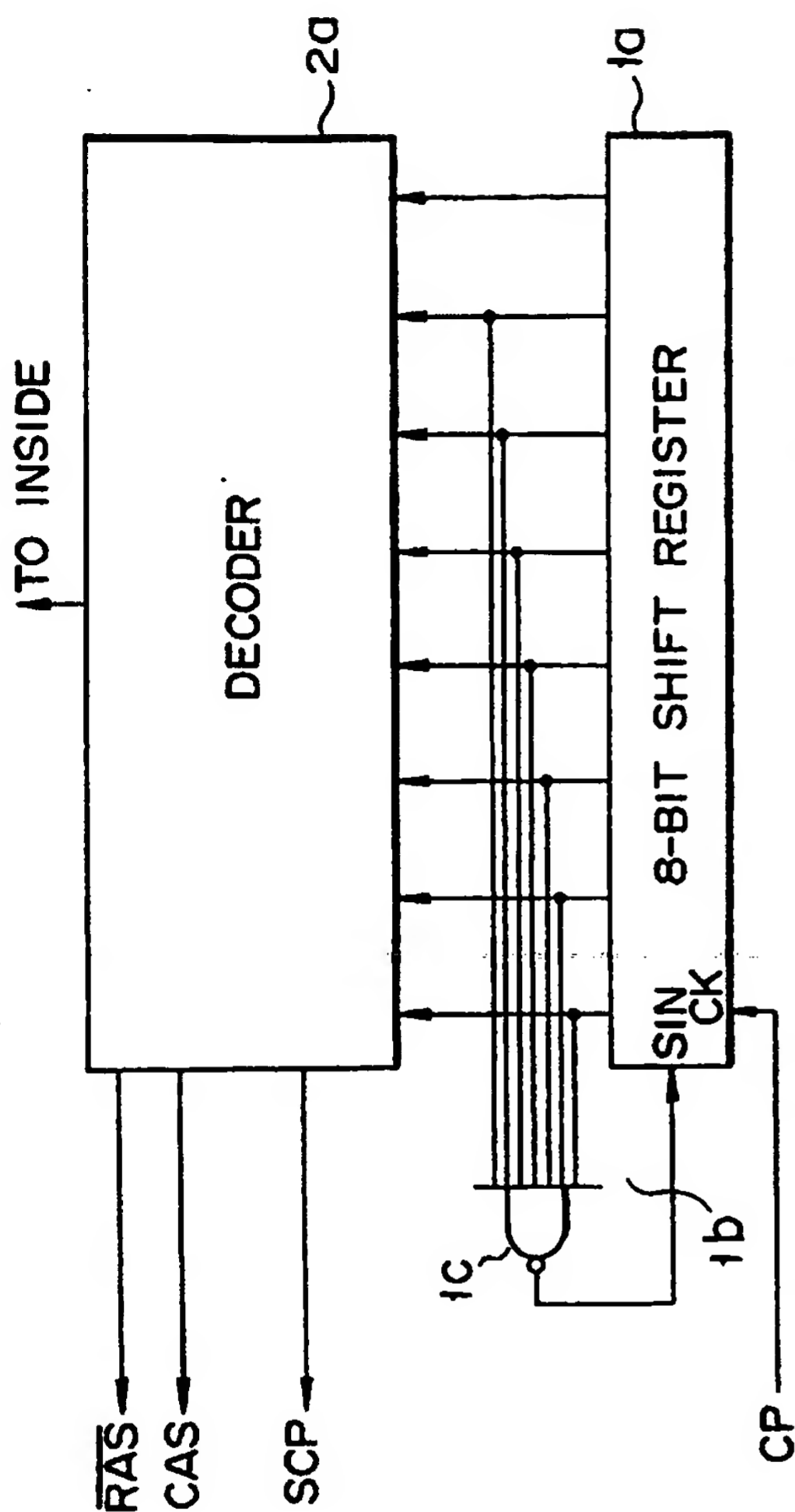


FIG. 3

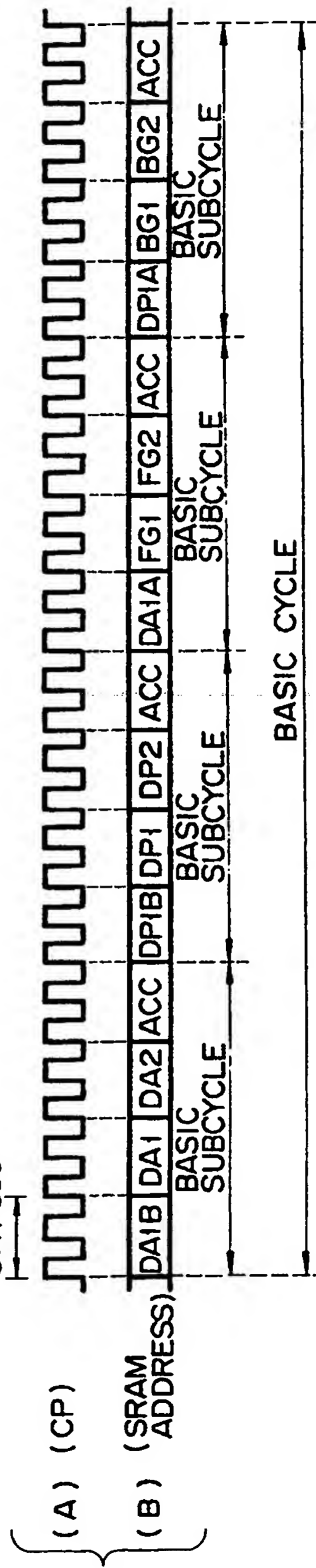
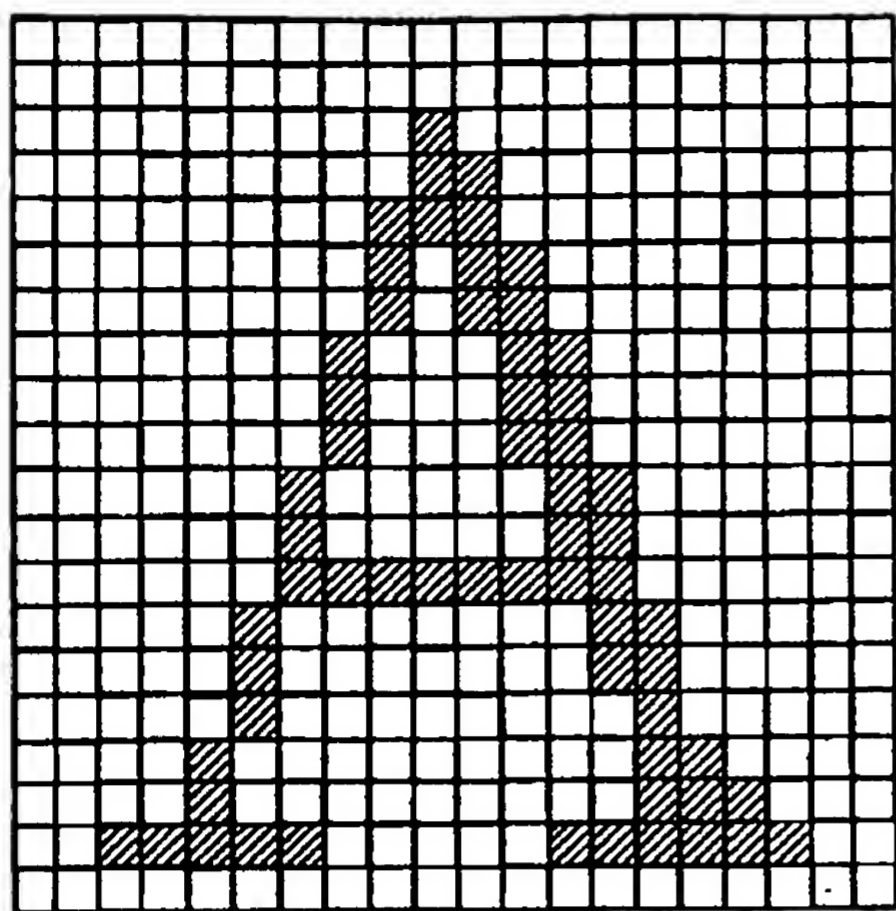
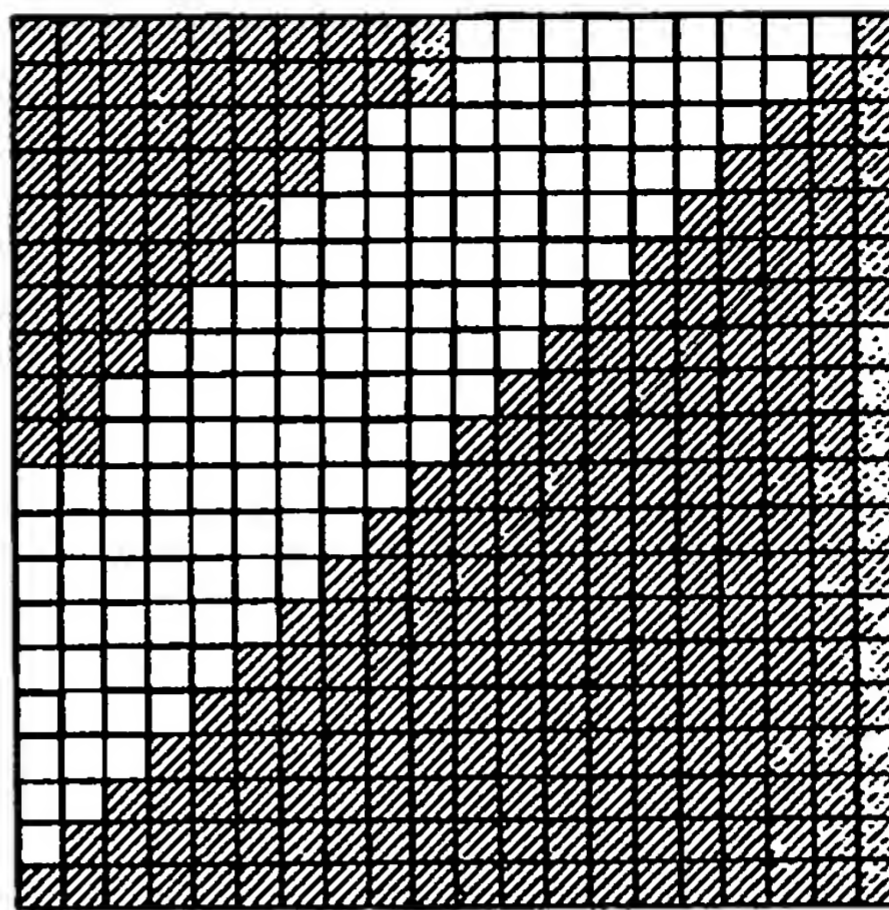


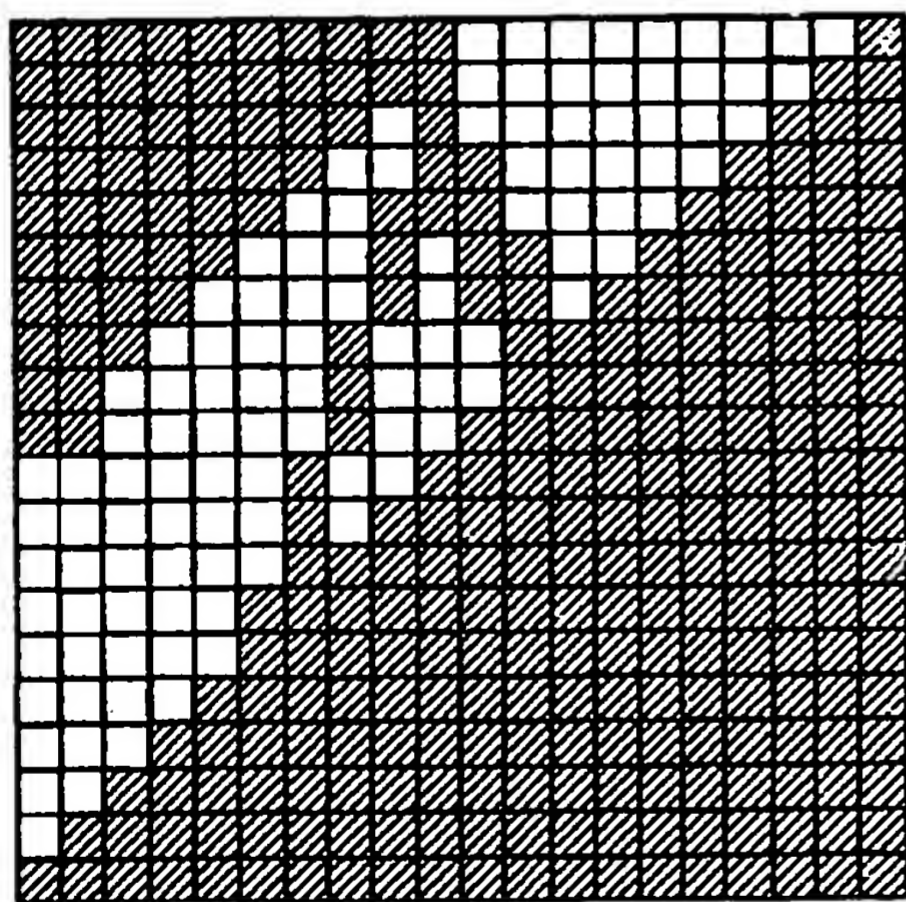
FIG. 4



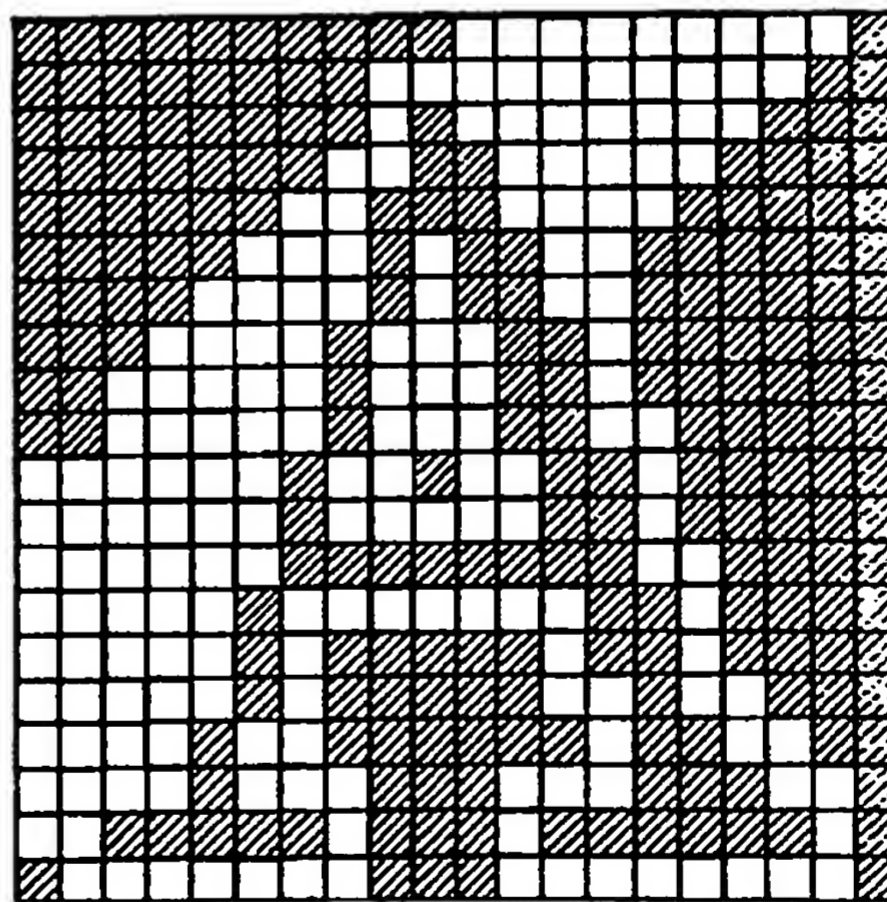
F I G. 5A



F I G. 5B



F I G. 5C



F I G. 5D

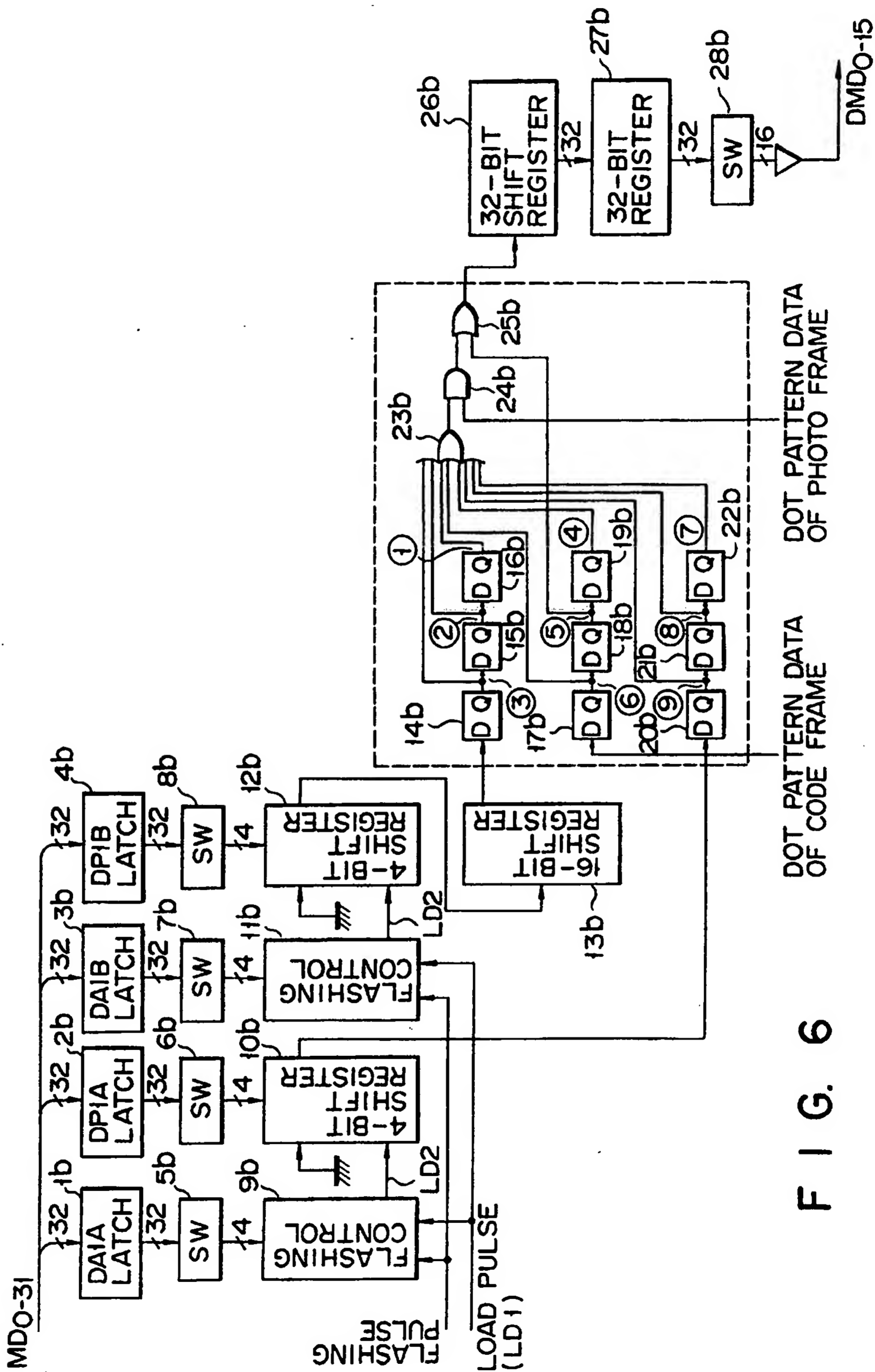


FIG. 6

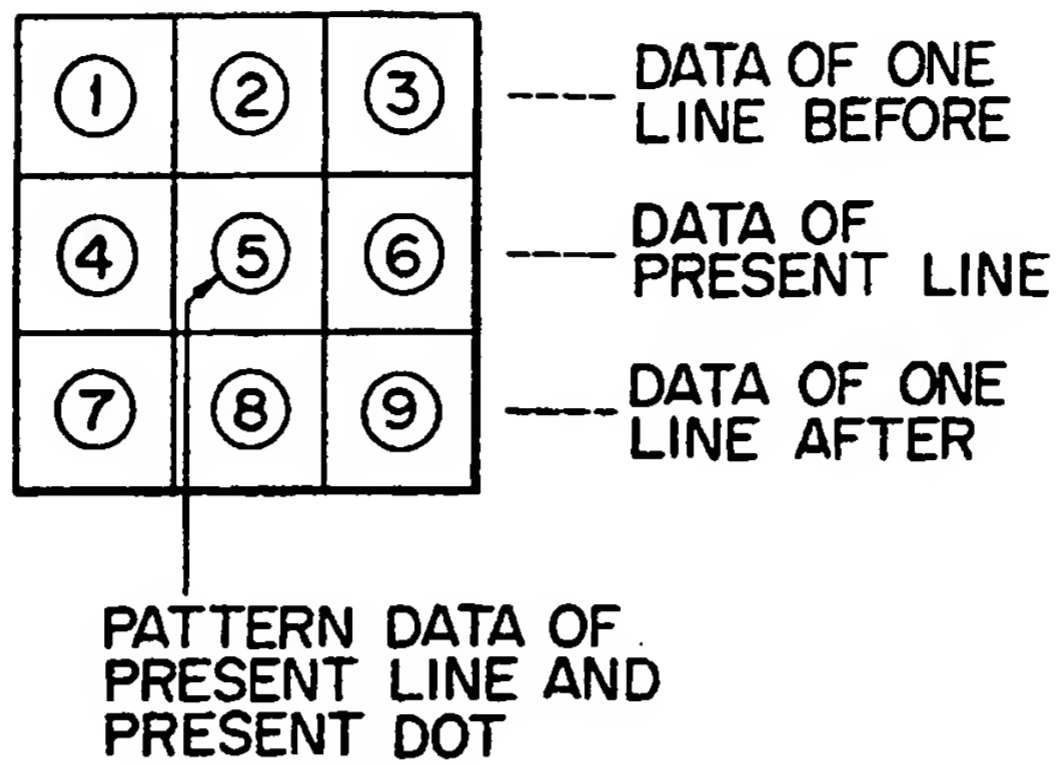


FIG. 7

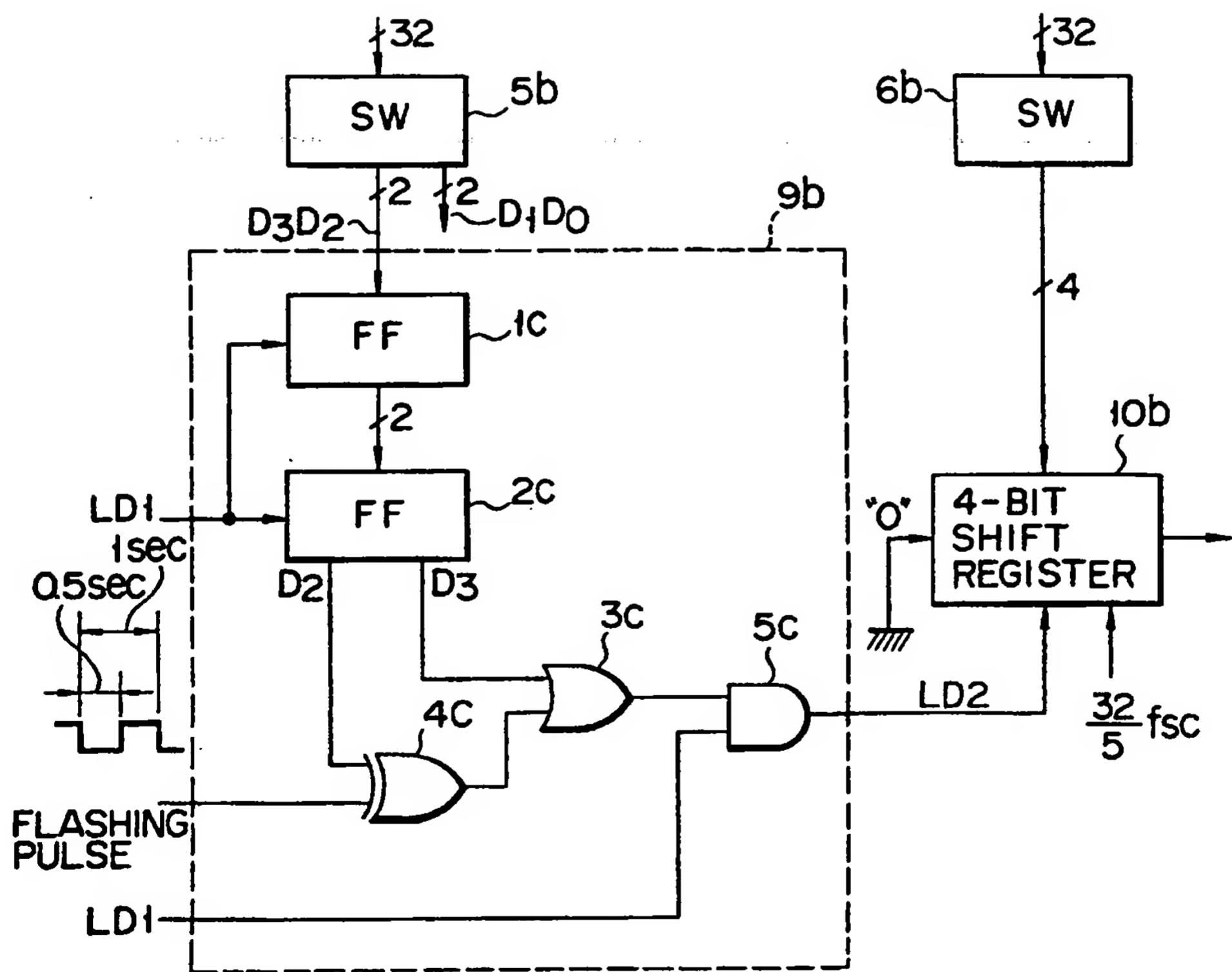
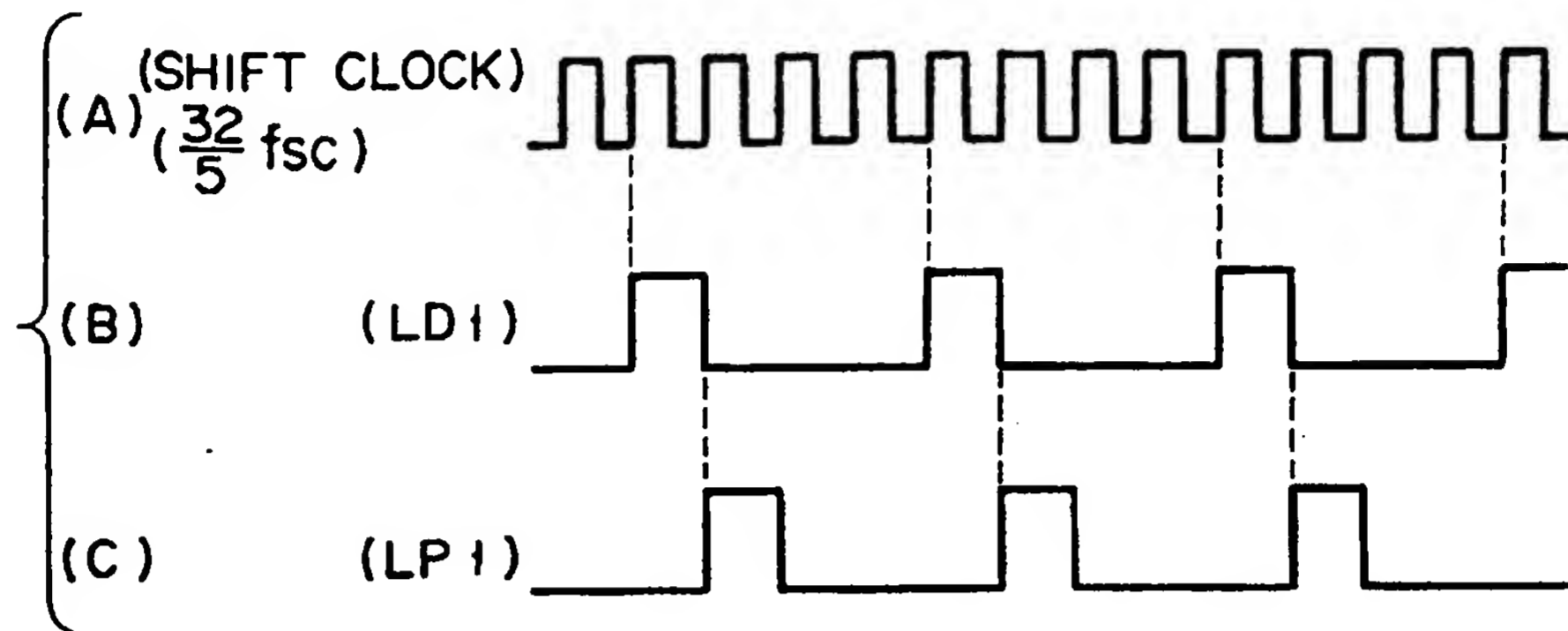
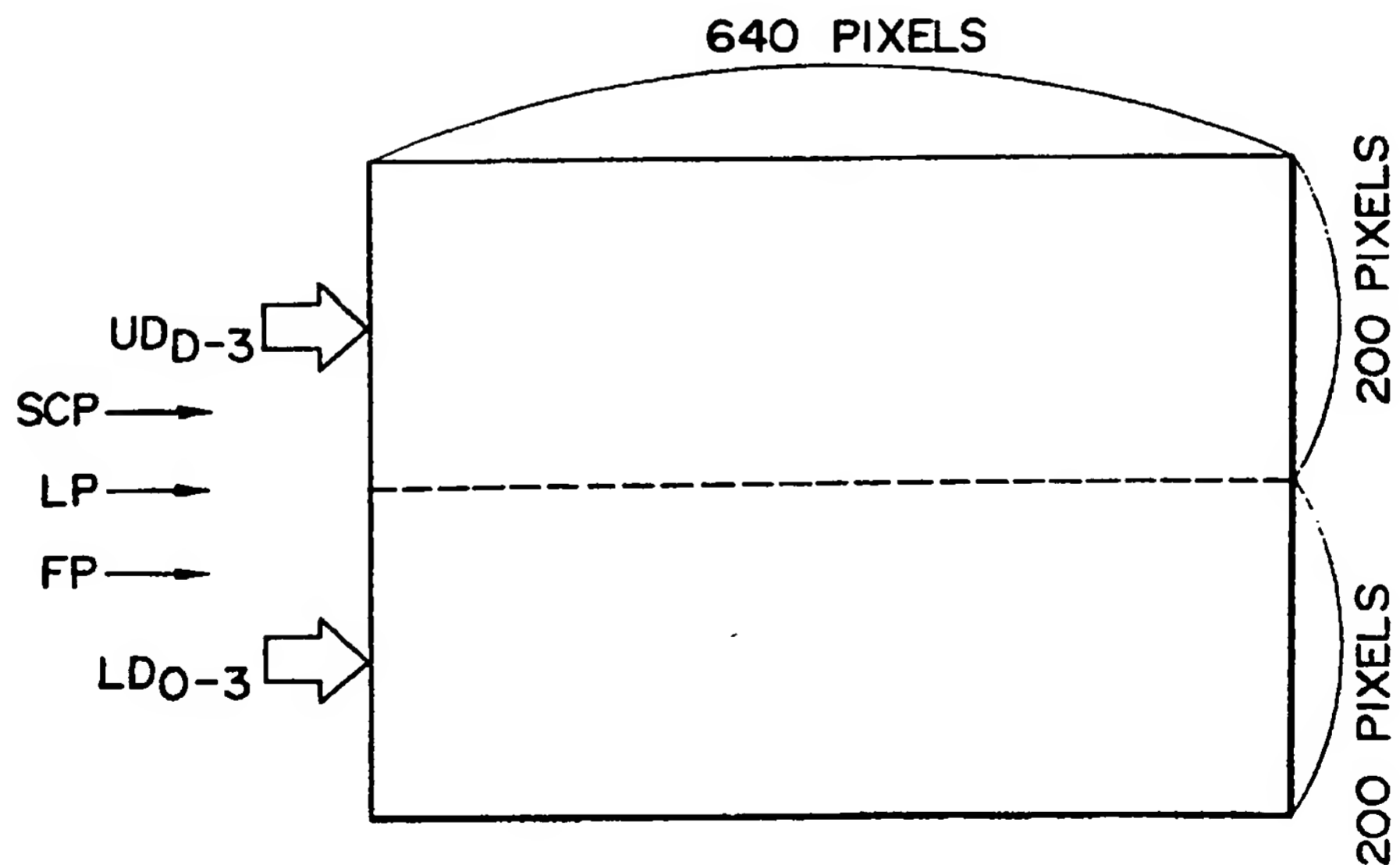


FIG. 8



F I G. 9



F I G. 10

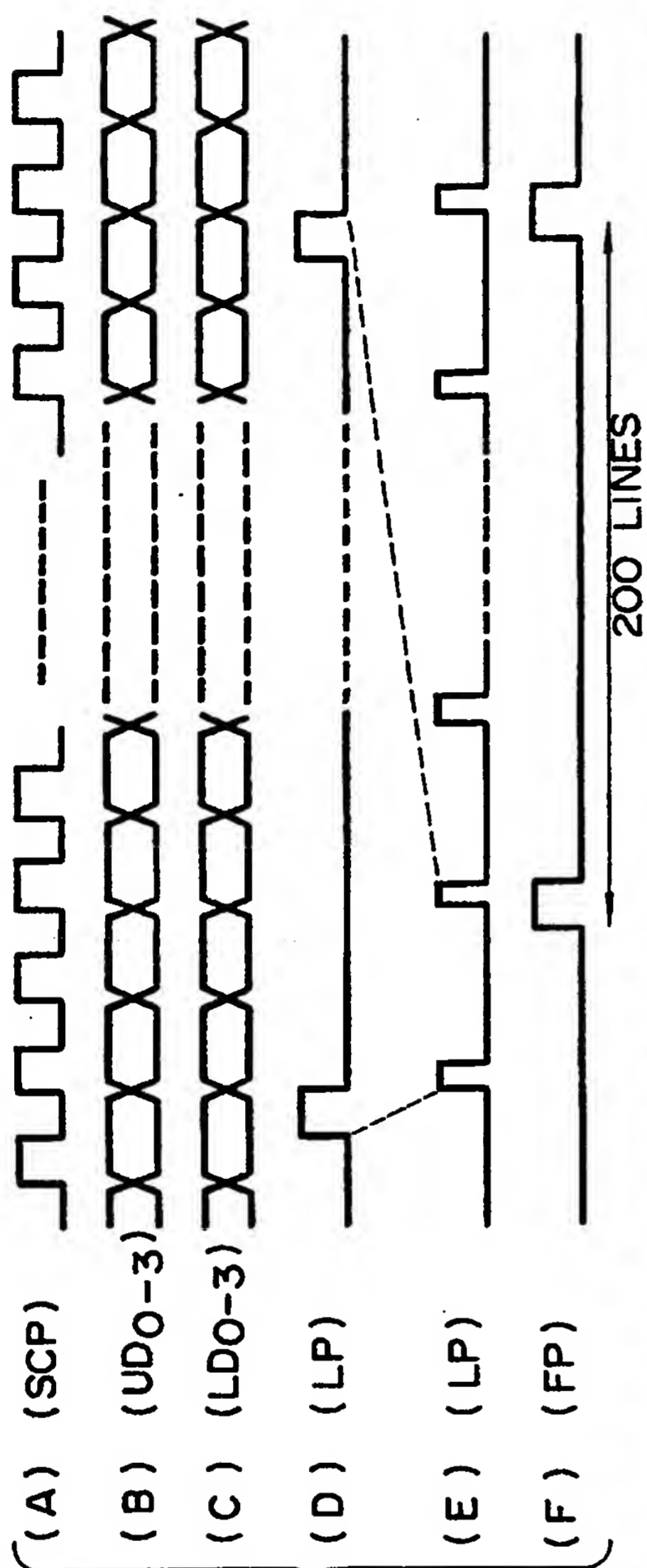


FIG. 11

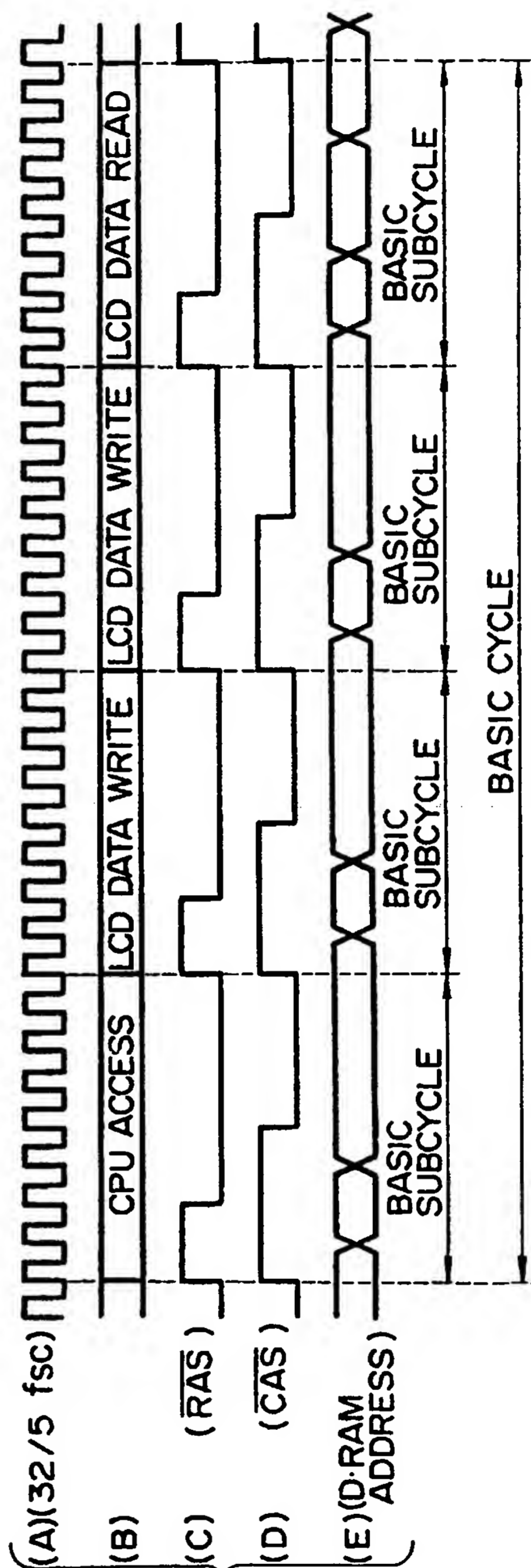


FIG. 12

"DISPLAY CONTROL APPARATUS FOR IMAGE DISPLAY SYSTEM"

The present invention relates to a display control device for an image display system, and more particularly to a display control device for use in an
5 image display system having an image memory, for instance, a videotex system such as the CAPTAIN or NAPLPS system, which stores transmitted image data in the image memory and reads the image data out of the image memory in sequence to display it on a display
10 device.

In a videotex system adapted for information delivery services using telephone lines, a cathode ray tube (CRT) of a television receiver is generally used as a display device for displaying transmitted information
15 visually.

In recent years liquid crystal display devices (LCDs) have widely been used as display devices for electronic equipment. The LCDs are classified into active-matrix type LCDs used with liquid crystal
20 television receivers and binary image type LCDs used with word processors and personal computers. The binary image type LCDs have, for example, 640 × 400 pixels each having two display states of on and off.

25 A liquid crystal television receiver using the active-matrix type LCDs can display images in colors and gradations like CRT display devices and may be used as

display devices for the videotex because of provision of video interface. On the other hand, the binary image type LCDs are not currently in use as display devices for the videotex. The reasons therefor may be the following

5 two:

(1) Image data used in the videotex system is composed of dot pattern data and color data and a frame is composed of two frames of a code frame and a photo frame. To display images on the binary image type LCDs
10 by using the image data for the videotex, predetermined data conversion processes would be required.

(2) The CRT and the binary image type LCD require different driving methods.

In view of the fact that equipment using the binary
15 image type LCDs is widely used, the use of the binary image type LCDs as display devices for the videotex system should be considered.

However, in using the binary type LCDs as display devices for the videotex the following two problems must
20 be taken into consideration.

A first problem may arise in constructing a videotex system which can use both active matrix type LCDs (or CRTs) and binary type LCDs. That is, if a display control device capable of controlling such
25 different types of display devices simultaneously were constructed, a separate display control section would generally be provided for each of the display devices.

More specifically, a display control section for an active matrix type LCD (or CRT) and a display control section for a binary type LCD would separately be connected to a central processing unit (CPU) for performing data processing such as data conversion on image data transmitted from an information center.

With such a construction, however, software used with the CPU would become complex because the CPU had to carry out different data conversion for two types of display devices. In hardware as well, the provision of two separate display control sections would increase circuit scale.

Next, a second problem may arise from the fact that the frames in the videotex system comprise two types of frame, one for code and the other for photo as described above, while the frames that the binary type LCDs handle comprise only one type of frame, and moreover the binary type LCDs can accommodate only dot pattern data indicative of brightness. That is, when dot pattern data of both of a code frame and a photo frame are displayed one above the other on a binary type LCD, they may not be distinguished from each other. This problem will arise both in the case where a videotex system that can accommodate the active matrix type LCDs (or CRTs) and the binary type LCDs is constructed and in the case where a videotex system that can accommodate only the binary type LCDs is constructed.

As described above, in the art of videotex systems, the development of a display control device is desired which is adaptable to two types of display devices, such as an active matrix type LCD (or CRT) and a binary type LCD, which are different from each other in image data structure and driving method. In this case there arise problems of complexity of software used and an increase in amount of hardware used. In addition, there is a problem of how to discriminate between a code frame and a photo frame in displaying image data of videotex on a binary type LCD.

It is accordingly an object of the present invention to provide a new and improved display control device for an image display system which accommodates two types of display devices with simplified software and a small amount of hardware.

It is another object of the present invention to provide a display control device which allows any type of display device to discriminate between two display frames, such as a code frame and a photo frame, which are necessary to display images.

According to an aspect of the present invention there is provided a display control device comprising:

first memory means;
second memory means; and
display control means comprising
(a) means for storing first data adapted to

a predetermined display device in said first memory means;

(b) means for reading the first data from said first memory means on a time division basis in sync with predetermined timing of display;

(c) means for converting the first data read out of said first memory means to second data adapted to a display device different from said predetermined display device;

(d) means for storing the second data in said second memory means; and

(e) means for reading the data stored in said second memory means out of said second memory in accordance with timing of display which is different from the predetermined timing of display.

Such an arrangement as described above can accommodate two different types of display devices with the aid of simple software and a small amount of hardware.

According to another aspect of the present invention, in order to control two types of display devices with simple software and a small amount of hardware, the present invention comprises an image memory, data conversion means, data writing means and data readout means for each of the display devices and is arranged such that, for display control of a first type of display device, incoming image data is converted to desired data

by the data conversion means and then written into the image memory by the data writing means, the data stored in the image memory is read out in sync with the timing of display of the corresponding display device by the data readout means, and, for display control of to a second type of display device, the data read out of the image memory for the first type of display device is converted to desired data by the data conversion means in sync with the timing of readout and then written into the image memory in accordance with the readout address of the image memory for the first type of display device, and the data stored in the image memory is read out in accordance with the timing of display of the second type of display device.

With such an arrangement, control sections for the respective display devices are provided not totally independently but in partially associated manner. Thus, complication of software and an increase in amount of hardware can be prevented.

That is, where a CPU is used as the means for converting incoming image data to image data for storage in the image memory, the CPU has only to carry out only the data conversion process for the first type of display device. Thus, the software for the CPU may be substantially the same as that used with a conventional display control device using only a CRT or active matrix type LCD. Although

two types of display devices are handled, the software may be simple.

Since the display readout address for the first type of display device is used as the write address for the second type display device, the need for write address generating means for the second type of display device is eliminated. The amount of hardware can be reduced as compared with a case where the write address generating means is provided for each of the two types of display devices.

Since the data conversion process by the CPU is performed only for the first type of display device, a section for monitoring the data conversion state may be provided only on the side of the first type of display device. The amount of hardware can thus be reduced as compared with a case where the monitoring section is provided for each of two types of display devices.

Furthermore, where a facility for erasing the image data stored in the image memory with hardware is provided, since data read out of the image memory for the first type of display device is written into the other image memory for the second type of display device, erasing of the image data stored in the image memory for the first type of display device will result in erasing of data stored in the image memory for the second type of display device. Hence, hardware erasing means may be provided only on the first type of display device.

The amount of hardware can be reduced as compared with the case where hardware erasing means is provided for each of two types of display devices.

According to still another aspect of the present invention, in order to identify two display frames, the invention first reads from image memory, for the first display frame, brightness data in the present display position and surrounding positions adjacent to the present display position and, for the second display frame, brightness data in the present display position, next decides whether or not the brightness data in the surrounding positions adjacent to the present display position for the first display frame have brightness, masks the brightness data in the present display position for the second display frame when they have brightness, and finally combines the masked output and the brightness data in the present display position for the first display frame.

With such an arrangement, since the brightness data for the second display frame surrounding the brightness pattern of the first display frame is masked, the brightness pattern is fringed, thus allowing the two display frames to be identified.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and

advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

The accompanying drawings, which are incorporated
5 in and constituted a part of the specification,
illustrate presently preferred embodiments of the invention and, together with the general description given above and the detailed description of the preferred
embodiments given below, serve to explain the principles
10 of the invention.

Fig. 1 is a block diagram of a display control device embodying the present invention;

Fig. 2 is a block diagram of the display control section of Fig. 1;

15 Fig. 3 is a schematic diagram of the basic timing generating section of Fig. 2;

Fig. 4 is a timing diagram explanatory of the operation of the display control section;

20 Figs. 5A to 5D are diagrams illustrating the operation of the display control section;

Fig. 6 illustrates a circuit arrangement of the LCD data converting section of Fig. 2;

Fig. 7 illustrates the operation of the LCD data converting section;

25 Fig. 8 shows a circuit arrangement of the flashing control section of Fig. 6;

Fig. 9 is a timing diagram explanatory of the

operation of the flashing control section;

Fig. 10 is a diagram explanatory of the operation of the display control section; and

Figs. 11 and 12 are timing diagrams explanatory of the operation of the display control section.

Preferred embodiments of the present invention will now be described in detail with reference to the accompanying drawings.

Reference will now be made in detail to the presently preferred embodiments of the invention as illustrated in the accompanying drawings, in which like reference characters designate like or corresponding parts throughout the several drawings.

Referring now to Fig. 1, there are shown a schematic arrangement of a videotex terminal CT including a display control device embodying the present invention and connection thereof to two types of display devices 9 and 10.

The embodiment of the present invention will be outlined here on the basis of the flow of data within videotex terminal CT with reference to Fig. 1.

In Fig. 1, a data signal transmitted over telephone lines L1 and L2 is applied to a bi-directional communication modulator/demodulator (MODEM) 2 via a network control unit (NCU) 1 for conversion from an analog signal to a digital signal. A central processing unit (CPU) reads data from modem 2 to decode it

according to videotex protocol and writes the decoded image data into a static random access memory (SRAM) 7 through a display control section 6.

5 Display control section 6 reads image data for a code frame and a photo frame from SRAM 7 in accordance with the display timing of a cathode ray tube (CRT) 9 to synthesize them into one frame of image data and convert them to R, G and B signals for application to CRT 9. Concurrently display control section 6 converts and
10 synthesizes dot pattern data for a code frame and a photo frame to data for a binary type LCD and writes it into a dynamic random access memory (DRAM) 8. In this case writing data into DRAM 8 is performed asynchro-
15 nously with the display timing of a liquid crystal display (LCD) 10 using cycle steal. On the other hand, display control section 6 reads display data for binary type LCDs from DRAM 8 for decoding in accordance with the display timing of binary type LCD 10 and supplies the decoded data to LCD 10.

20 In Fig. 4, reference numeral 4 denotes a read only memory (ROM) for storing software for the videotex terminal, and 5 denotes a DC power supply for generating various DC voltages for the above sections 1 to 10.

25 As can be seen from the foregoing, from the standpoint of software, this embodiment is required only to write image data into SRAM 7 so as to allow display data to be applied to CRT 9 and LCD 10 in

real time. Thus the burden imposed on software does not increase.

Referring now to Fig. 2, display control section 6 is functionally divided into five sections (A), (B),
5 (C), (D) and (E).

Section (A) is a timing generating section which is composed of a basic timing generating subsection (A-1) for generating basic timing signals, an H signal generating subsection (A-2) for generating various
10 timing signals including a horizontal sync signal (H.SYNC) and a vertical sync signal (V.SYNC) for CRT 9, and a V signal generating subsection (A-3). More specifically, basic timing generating subsection (A-1) produces basic timing signals for CRT 9 and LCD 10 and,
15 as shown in Fig. 3, is comprised of a ring counter 1a, consisting of an 8-bit shift register 1b receiving a basic clock CP and a NAND circuit 1c, and a decoder 2a for providing various timing signals to the inside and the outside of the display control section.

20 Section (B) is an address generating section for providing addresses of SRAM 7, which comprises a Y address generating subsection (B-1) for generating addresses along a vertical line of a display screen, a CPU address latch subsection (B-2) for latching
25 addresses (A0-16) from CPU 3 used when CPU 3 writes data into or reads data from SRAM 7, and an address switching subsection (B-3) for providing data addresses

on a time division basis.

Y address generating subsection (B-1) outputs Y addresses of a code frame and a photo frame separately. This is because the photo frame is scrolled vertically in the videotex system. X addresses, which are addresses along a horizontal line of the display screen, are applied from H signal generating subsection (A-2) to address switching subsection (B-3).

Here image data necessary for the videotex system comprise dot pattern data DP1, foreground color data FG1, background color data BG1 and flashing data for a code frame (those data are simply abbreviated to DP1, FG1, BG1 and DA1 hereinafter), and dot pattern data DP2, foreground color data FG2, background color data BG2 and flashing data DA2 for a photo frame (those data are abbreviated to DP2, FG2, BG2 and DA2 hereinafter). There are further required dot pattern data DP1B and DP1A and flashing data DA1B and DA1A of a code frame for lines one line before and after the present line (hereinafter abbreviated to DP1B, DA1B: one line before, and DP1A and DA1A: one line after) so as to define the boundaries the code frame and the photo frame displayed on LCD 10 as will be described later. Hence display control section 6 has to read 12 types of data from SRAM 7 for image display on LCD 10. Access to SRAM 7 from CPU 3 also must be performed at regular intervals.

Assuming that LCD 10 has 640 × 400 pixels,

it can accommodate double density display. Since
496 × 408 pixels are required for double density
display, LCD 10 is short by 8 pixels in the number
of pixels along a vertical line. This can be solved
5 by setting the number of pixels of a header not to
24 pixels which are general in the CAPTAIN (character
and pattern telephone access information network) system
but to 16 pixels. Hence the present embodiment is
directed to the double density display adapted to rank 3
10 of the videotex system. Taking a double scan monitor
which is double in frequency the NTSC system as CRT 10
for double density display, the frequency of display
clock (basic clock) CP will be 32/5 fsc (about 43 nsec).
As SRAM 7 use may be made of a commercial available
15 static random access memory having an access time of 85
nsec. Then an access time for one piece of data may be
set to a period of time (about 87 nsec) which is double
the cycle period of display clock CP. For efficient
utilization of the memory the above data require reading
20 on a time division basis. For further securing the
access time which is double the cycle period of display
clock CP in addition to the fact that 12 types of
display data are required and access by CPU 3 is made at
a predetermined cycle, it is most desirable that the
25 data bus of SRAM 7 have 32 bits (MD0-31).

Fig. 4 shows a relationship between a basic cycle
and basis subcycles for SRAM 7 in the case of 32-bit

data bus. ACC represents a period in which an address
used by CPU 3 to access SRAM 7 is output, which is
referred to as an ACC period hereinafter. DA1B, DA1,
DA2,... and so on represent periods in which addresses
5 for respective pieces of data of the code and photo
frames are output. The basic cycle of SRAM 7 is
composed of four basic subcycles generated by basic
timing generating section (A-1). In a double scan
mode, one horizontal cycle comprises cycles of 728
10 display clocks CP. Thus one horizontal cycle is
composed of 91 basic subcycles.

Referring back to Fig. 1, the (C) section is
an access/erase section including a subsection
adapted to perform access control when CPU 3 writes
15 data into or reads data from SRAM 7 and a subsection
adapted to erase a displayed frame by means of hardware.
More specifically, hardware erase subsection (C-1)
is responsive to application from CPU 3 thereto of a
command for erasing a displayed frame such as a code
20 frame or a photo frame to initiate erasing the dis-
played frame. The hardware erasing is carried out
by using display addresses output from address
generating section (B). Hardware erase subsection
(C-1) drives data converting subsection (C-2) to
25 output erasing data onto SRAM data bus (MD0-31) and
drives SRAM access control & WAIT control subsection
(C-5) to provide write pulses (WE0-3) while address

generating section (B) generates display addresses for pieces of data.

Write data register (C-3) is adapted to hold write data which is written into SRAM 7 by CPU 3. When write
5 data register (C-3) is loaded with write data via CPU data bus D0-7, the data is written into SRAM 7 via SRAM data bus MD0-31 during an ACC period shown in Fig. 4. The write pulses used at this point are supplied from SRAM access control and WAIT control subsection (C-5).
10 The addressing of SRAM 7 is carried out by outputting a CPU address held by CPU address latch (B-2) onto SRAM address bus MA0-4. Read data register (C-4) is adapted to store read data which is read from SRAM 7 by CPU 3.

SRAM access control & WAIT control subsection (C-5)
15 is adapted to control writing into and reading from SRAM 7 by CPU 3. SRAM access control & WAIT control subsection (C-5) receives various control signals from CPU 3, such as a clock (CPUCK) of CPU 3, an identification signal (IO/M) for identifying an IO area and a memory area, a
20 read signal (RD), a write signal (WR) and a signal (RAMCS) for indicating an address space of SRAM 7, detects CPU access to SRAM 7, applies a READY signal to CPU 3 and causes it to enter the wait state so that SRAM 7 may be accessed during a predetermined ACC period.
25 SRAM access control & WAIT control subsection also provides four write signals WE0-3 to be applied to SRAM 7.

The (D) section is a decoder section which decodes image data for photo and code frames read out of SRAM 7 for synthesis into one frame of image data and conversion to R, G and B signals. R, G and
5 B signals are converted to four bit digital data R0-3, G0-3 and B0-3 by a color lookup table RAM (referred to as LUTRAM hereinafter) and then converted to analog signals by an D/A converter not shown for application to CRT 9.

10 RGBC decoder (D-1) is an RGB decoder for a code frame adapted to decode DP1, DA1, FG1 and BG1 read out onto SRAM data bus D0-31 from SRAM 7 by CPU 3 and provides an 4-bit entry address to LUT control subsection (D-4). At the same time decoder (D-1) provides
15 dot pattern data DP1 of a code frame (for the current line) to a LCD data converter (D-3). RGBP decoder (D-2) is a RGB decoder for a photo frame adapted to decode DP2, DA2, FG2 and BG2 read out onto SRAM data bus D0-31 from SRAM 7 by CPU 3 and provides a 4-bit entry address
20 to LUT control subsection (D-4). At the same time decoder (D-2) provides dot pattern data DP2 of a photo frame (for the current line) to a LCD data converter (D-3).

CTRIP register (D-5) and PTRIP register (D-6) are
25 adapted to specify which of the entry addresses become transparent and store transparent data of code and photo frames, respectively, which are supplied from CPU 3 via

CPU data bus D0-7. The entry addresses from decoders (D-1) and (D-2) and the transparent data stored in registers D-5 and D-6 are applied to LUT control subsection D-4. LUT control subsection D-4 decides
5 the transparent of a code frame according to the predetermined priority and supplies either entry addresses of the code frame or those of the photo frame to LUTRAM D-7. That is, if the code frame is not transparent, the entry address of the code frame
10 is selected. If the code frame is transparent, on the other hand, the entry address of the photo frame is selected. LUTRAM D-7 provides R, G and B data each of 4 bits corresponding to the entry address. The R, G and B data are applied to a switch subsection D-10
15 which selects either the R, G and B data or R, G and B data for a raster color for application to a BLK converter D-11. A switch signal to select either the R, G and B data from LUTRAM D-7 or the raster R, G and B data is provided from LUT control subsection D-4. In
20 response to the switch signal switch subsection D-10 selects the raster R, G and B data when the code frame and the photo frame are both transparent or when they are out of the display area.

Finally, BLK converting subsection D-11 converts
25 the R, G and B data to all 0s during a blanking interval and outputs them as R0-3, G0-3 and B0-3. LUT data register D-8 is a register which is loaded with write

data when CPU 3 writes it into LUTRAM D-7. Raster color register D-9 is a register which stores R, G and B data (each of 4 bits) of a raster which is out of the display area.

5 LCD data converting subsection D-3 is adapted to produce display data for LCD 10 from dot pattern data of code and photo frames read out of SRAM 7 to display an image on CRT 9. Here an LCD having two states of ON and OFF is used as LCD 10. Hence, in order to
10 display data for use in the videotex system having two types of frames on binary type LCD 10, the data requires some processing. The videotex system has color data as well as dot pattern data of pixel information. Taking the fact that the videotex system is a system for
15 receiving information into consideration, only dot pattern data of each of the code and photo frames will allow information to be visually displayed. Therefore, the identification of each of two types of frames is left to consideration.

20 Fig. 5C shows the logical sum of dot pattern data of a code frame of Fig. 5A and dot pattern data of a photo frame of Fig. 5B. As can be seen from this example, when two pieces of data are simply ORed to superimpose the code frame upon the photo frame,
25 they cannot be distinguished from each other. In the present embodiment, therefore, the dot pattern of the code frame is fringed as shown in Fig. 5D so as to allow

two pieces of data to be distinguished from each other.
That is, in Fig. 5C, blank areas each of one dot are
provided around the dot pattern data of the code frame,
the dot pattern data of the photo frame corresponding
5 to the blank areas are masked and the resultant dot
pattern data of the code and photo frames are ORed.
Hence the blank areas each of one dot are created along
the boundary between the code frame data and the photo
frame data, thus permitting discrimination between two
10 pieces of data.

In Fig. 6, there is illustrated a specific arrange-
ment of LCD data converting subsection D-3. Dot pattern
data DP1B and DP1A and flashing data DA1B and DA1A of a
code frame for lines of one line before and after the
15 present line are sequentially read out of SRAM 7 at
times shown in Fig. 4 and then held in latch circuits
4b, 2b, 3b and 1b, respectively. Each of succeeding
switch circuits 5b, 6b, 7b and 8b converts the 32-bit
latched data in a corresponding latch circuit to 4-bit
20 data in miniblock (4 dots x 4 dots) units. The con-
verted dot pattern data DP1A and DP1B are supplied to
4-bit shift registers 10b and 12b, respectively.
Flashing controller 9b and 11b control the supply of
a load pulse LD2 to 4-bit shift registers 10b and 12b in
25 accordance with flashing data DA1A and DA1B and a
flashing pulse. A 16-bit shift register 13b compensates
for the time difference in the data resulting from

a difference in the timing of readout between dot pattern data DPlB of one line before and dot pattern data DPlA of one line behind, that is, establish synchronization between DPlA and DPlA.

5 In Fig. 6, a portion enclosed with dotted lines
is adapted to reduce one-dot data around the dot pattern
data of a code frame to blank data, to mask the dot
pattern data of a photo frame and to OR the masked dot
pattern data with the dot pattern data of the code
10 frame. As shown in Fig. 7, reducing one-dot data around
the dot pattern data (5) of the code frame and masking
the dot pattern data of the photo frame means that, if
an array of 3 x 3 pixels surrounding the dot pattern
data (5) of the present dot on the present line of the
15 photo frame has dot pattern data of the code frame
representing brightness, then the dot pattern data 5 of
the photo frame is masked. More specifically, if at
least one of pixels (1), (2), (3), (4), (6), (7), (8), (9) has
dot pattern data, the dot pattern data on the center
20 pixel (5) is masked. Hence dot pattern data of a code
frame corresponding to three lines of the present line
and the upper and lower lines need to be read out.

 In Fig. 6, D flip-flops 14b to 22b are adapted to
latch data of nine pixels (1) to (9) of Fig. 7, respec-
25 tively. An 8-input NOR 23b decides whether at least one
of eight pixels of Fig. 7, exclusive of pixel (5), have
dot pattern data or not. In accordance with the result

of this decision the dot pattern data of the photo frame is masked. An 2-input OR gate 25b Ors the masked output with the dot pattern data of the code fame.

The data synthesized in this way is then converted
5 to 32-bit data by a 32-bit shift register 26b and a
32-bit register 27b. The 32-bit data is divided into
two pieces of 16-bit data for time-division multiplexing
by a switch circuit 28b and the resulting 16-bit data is
applied to data bus DMD0-15 of DRAM 8. Writing the
10 16-bit data into DRAM 8 is carried out by section (E) of
Fig. 2.

It is to be noted here that the flashing control of
the dot pattern data DPlB and DPlA on the lines of one
line before and after the present line is performed for
15 varying the fringing state in accordance with the
flashing state. That is, if no flashing control were
performed for the dot pattern data DPlB and DPlA, the
fringing would be done even in the flashing-off state.
As a result, in the example of Figs. 5A to 5D, an image
20 in which "A" is excluded from Fig. 5D would be obtained.
As in the present embodiment, on the other hand, if the
flashing control is performed for the dot pattern data
DPlB and DPlA, the fringing will not be done when the
flashing is off. Consequently, an image in which "A" is
25 excluded from Fig. 5C, namely, an image of Fig. 5B which
is to be displayed primarily can be obtained.

It is needless to say that, although not shown in

Fig. 6, the dot pattern data DP1 and DP2 of code and photo frames for the present line are subjected to the flashing control.

5 A description will now be given of a specific arrangement of flashing controllers 9b and 11b with reference to Figs. 8 and 9A to 9C. Fig. 8 illustrates a circuit arrangement of flashing controller 9b, while Figs. 9A to 9C are timing charts explanatory of the operation of the circuit of Fig. 8.

10 In Fig. 8, 4-bit flashing data DALA is output from switch circuit 5b as described above. When the bits of flashing data DALA are represented by D3, D2, D1 and D0, the high-order two-bit data D3 and D2 are used for flashing control. More specifically, the
15 most significant bit data D3 is used to specify whether flashing control is to be done or not. D3 = 1 when flashing control is not to be done, otherwise D3 = 0. Data D2 is used to specify either positive-phase flashing or opposite-phase flashing. D2 = 0 for
20 positive-phase flashing, while D2 = 1 for opposite-phase flashing. Data D3 and D2 are applied to an OR circuit 3c and an EXCLUSIVE OR circuit 4c, respectively, via timing flip-flop circuits 1c and 2c.

Assuming now that D3 = 1, the output of OR circuit
25 3c is always "1". Thus a load pulse LD1 passes through an AND circuit 5c to enter a 4-bit shift register 10b as a load pulse LD2. Consequently, 4-bit dot pattern data

DPlA is loaded from switch circuit 6b into shift register 10b. The data is output serially one bit at a time in accordance with shift clocks (display clocks) shown in Fig. 9A.

5 As described above, when D3 = 1, load pulse LD2 is applied to shift register 10b irrespective of a flashing pulse supplied to EXCLUSIVE OR circuit 4c with the result that the flashing is not performed.

10 Next, when D3 and D2 are both 0, the flashing pulse is applied to AND circuit 5c via EXCLUSIVE OR circuit 4c and OR circuit 3c. In this case, therefore, load pulse LD1 passes through AND circuit 5c only when flashing pulse is 1 to serve as load pulse LD2. When the flashing pulse is 0, on the other hand, AND circuit 5c produces no load pulse LD2. Namely, when the flashing pulse is 1, dot pattern data DPlA is loaded into 4-bit shift register 10b for conversion to serial data. On the other hand, when the flashing pulse is 0, dot pattern data DPlA is not loaded into 4-bit shift
15 register 10 with the result that 0s are shifted through shift register 10b. This results in masking of dot pattern data DPlA output from switch circuit 6b.
20

25 As described above, when data D3 and D2 are both 0, the positive-phase flashing state results in which the flashing is off when the flashing pulse is 1 and the flashing is off when the flashing pulse is 0.

For example, the flashing pulse has a cycle period

of one second and a duty factor of 50 %. Thus the flashing is switched at 0.5-sec intervals.

Finally, when D3 and D2 are both 0, EXCLUSIVE OR circuit 4c serves as an inverter so that the flashing pulse is inverted. In this case, therefore, it is when the flashing pulse is 0 that load pulse LD2 is applied to 4-bit shift register 10b. As a result, the opposite-phase flashing state is obtained in which the flashing is off when the flashing pulse is 1, while the flashing is on when the flashing pulse is 0.

Latch pulse LP1 for flip-flop circuits 1c and 2c and load pulse LD1 are each generated every four shift clocks.

The arrangement of flashing controller 9b was described above. The other flashing controller 11b is identical in arrangement to flashing controller 9b and thus its description is omitted.

Referring back to Fig. 2, the (E) section is a DRAM control section for carrying out the general control of DRAM 8. An LX counter E-1 and an LY counter E-2 produce various control signals necessary to drive LCD 10. Here an interface to LCD (module) 10 will be described briefly. LCD 10 with 640 x 400 pixels is usually driven in two parts. That is, 400 pixels along a vertical line are divided into two parts each of 200 pixels. Four-bit data UD0-3 and four-bit data LD0-3 are simultaneously applied to the upper 640 x 200 pixel part and the lower

640 x 200 pixel part, respectively. SCP is a clock for the 4-bit data, LP is a signal representing a cycle of LCD 10 along its horizontal line, and FP is a signal representing a cycle of LCD 10 along its vertical line.

5 The timing diagrams of these signals are shown in Figs. 11A to 11F. With LCD 10 a frame rate of about 70 Hz is standard. If the frame rate were slower, the flicker would become noticeable, while if the frame rate were faster, the liquid crystal medium could not
10 respond. In the present embodiment, the basic clock is 32/5 fsc (22.9 MHz). Assuming that the cycle period of clock pulse SCP is equal to the basic cycle period (eight times the 32/5 fsc clock cycle) and one horizontal line covers not 640 pixels but 768 pixels, then the
15 frequency of signal LP becomes about 14.915 KHz. Since 200 LP signals corresponds to one cycle of signal FP defining one cycle of vertical scan, the frequency of signal FP becomes about 74.57 Hz (roughly 70 Hz). From the foregoing, assuming the basic cycle to be a minimum
20 unit, LX counter E-2 may be a modulo-192 counter.

Although LY counter E-2 is a modulo-200 counter, since the header area of LCD 10 comprises not 24 lines but 16 lines as described above, the LY counter is preferably a modulo-200 counter from 8 to 207. Thus, the header
25 area corresponds counts of 8-23, and the display area corresponds to counts of 24-207 so that the display addresses for LCD 10 conveniently coincide with the

display addresses for CRT 9.

DRAM address control & LCD control subsection E-3 comprises a portion for producing addresses to DRAM 8 and a portion for producing various control signals to
5 LCD 10. The control signals for LCD 10 include horizontal and vertical scan signals LP and FP, which are produced by decoding counts of LX counter E-1 and LY counter E-2. The addresses to DRAM 8 comprise addresses used in writing dot pattern data
10 which are read out of SRAM 7 and synthesized into DRAM 8, the addresses used when CPU 3 accesses DRAM 8 to read data therefrom and write data thereinto, and the display addresses used for displaying data on LCD 10. The write addresses from SRAM 7 to DRAM 8
15 are applied from address switcher B-3 to DRAM address control & LCD control subsection E-3. The addresses for access to DRAM are applied from D-RAM access control subsection E-4 to DRAM address control & LCD control subsection E-3. The display addresses are applied from
20 LX counter E-1 and LY counter E-2 to DRAM address control & LCD control subsection E-3.

The timing diagrams of the DRAM addresses and RAS and CAS signals are shown in Figs. 12A to 12E. The CPU access period of Fig. 12B is a period during which CPU 3
25 reads from or write into DRAM 8. In this period the addressed from CPU 3 are latched by DRAM access control subsection E-4 for subsequent application to DRAM

address control & LCD control subsection E-3. Data writing by CPU 3 into DRAM 8 is carried out in units of 8 bits and 8-bit data is transferred to DRAM data bus DMD 0-7 or DMD 8-15 according to its address. At the same time write pulses DWR0 and DWR1 are made active according to the address. DWR0-1 is provided from DRAM access control subsection E-4. LCD data write is repeated two times consecutively. If CPU 3 detects the completion of the process of LCD data converting subsection D-3, data is written into DRAM 8 during those periods. The 32-bit data produced by LCD data converting subsection D-3 during those periods time divided into two parts each of 16 bits and output onto DRAM data bus DMD0-15. The write address is applied from address switcher B-3 to DRAM address control & LCD control subsection B-3 and then output onto DRAM address bus DMA0-8 as a row address and a column address in accordance with the timing shown in Fig. 10. At the same time the write pulses DWR0-1 go active together. It is only during data of the display area, exclusive of the header area, are processed by LCD converting subsection D-3 that automatic writing of data is performed. The data of header area are directly written into DRAM 8 by CPU 3.

25 The CPU data read period is a period during which data are read out of DRAM 8 so as to display the data on LCD 10. Since, in this case, data divided into two

upper and lower parts are needed to be applied simultaneously to LCD 10, two pieces of 16-bit data are needed to be read out during this period. To this end the present embodiment utilizes the static column mode.

5 That is, addresses along a vertical line (counts of LY counter E-2) are supplied as column addresses, the first addresses being those of 8-207 lines and the next addresses being addresses of 208-407 which are offset by 200 with respect to 8-207. Hence, data for the
10 upper half of LCD 10 are read out by row addresses and the first column addresses, and data for the lower half of LCD 10 are read by the second column addresses. Each piece of 16-bit data is applied to LCD data converting subsection E-5 and converted to data units each of 4
15 bits (UD0-3, LD0-3) for subsequent application to LCD 10. Since the writing of data from SRAM 7 into DRAM 8 is carried out during 32 clock periods of $32/5$ fsc, failure in data writing will never occur.

As described above, the present embodiment is
20 provided with CPU 3 for processing image data to be displayed, SRAM 7 for storing image data for CRT 9, DRAM 8 for storing image data for binary type LCD 10 and display control section 6 for controlling SRAM 7 and DRAM 8 in partial association with each other. For
25 display control for CRT 9, display control section 6 stores image data resulting from conversion of transmitted image data to data for CRT 9 by CPU 3

therein, writes it into SRAM 7 and then reads out the data stored in SRAM 7 in sync with the display timing of CRT 9. For display control for LCD 10, on the other hand, display control section 6 converts image data read out of SRAM 7 to be displayed on CRT 9 data for LCD 10 in sync with the timing of readout of the image data, writes it into DRAM 8 in accordance with the readout address of SRAM 7, and reads it out of DRAM 8 in sync with the timing of display of LCD 10.

According to such an arrangement, display control section 6 need not be provided for CRT 9 and LCD 10 separately and has only to carry out controls for CRT 9 and LCD 10 in partially associated manner. Thus, the complication of software and an increase in amount of hardware can be prevented.

More specifically, with respect to the prevention of complication of software, CPU 3 has only to carry out data conversion process for CRT 9. Thus, the software for CPU 3 may be substantially the same as software for a display control device for controlling only a conventional CRT or active matrix LCD and may be simple irrespective of controlling both CRT 9 and LCD 10.

Next, the reasons for the prevention of an increase in amount of hardware will be listed as follows:

① Since the address of data read out of SRAM 7 for display is used as the address of DRAM 8 into which the data is to be written, the need for an address

generating means on the LCD side is eliminated.

② Since CPU 3 performs data conversion process on the CRT side, a circuit for monitoring the data conversion processing state may be provided only on the CRT side.

③ In an attempt to erase image data stored in an image memory with hardware, erasing image data in SRAM 7 will result in erasing data stored in DRAM 8 because data read from SRAM 7 is written into DRAM 8. Thus, hardware erasing subsection C-1 may be provided only the CRT side.

④ Since SRAM 7 and DRAM 8 are made equal to each other in the basic cycle for access thereto, the need for a buffer circuit for preventing failure in writing data into DRAM 8 is eliminated. In writing data read out of SRAM 7 into DRAM 8, the present invention reads dot pattern data (① to ⑨ of Fig. 7) of the present dot and surrounding display dots in the case of a code frame, reads the dot pattern data (⑤ of Fig. 7) of the present dot in the case of a photo frame, decides whether or not the dot pattern data of surrounding dots of the present dot have brightness, masks the dot pattern data of the present dot (⑤ of Fig. 7) when they have brightness, and finally combines the masked output and the dot pattern data of the present dot (⑤ of Fig. 7) of the code frame together.

According to the above arrangement, because the

dot pattern data of the photo frame surrounding the
dot pattern of the code frame is masked, the code
and photo frames can be distinguished from each other
in spite of the fact that the code and photo frames
5 are displayed one above the other.

In this case, the dot pattern data DP1B and DP1A
(①, ②, ③, ⑦, ⑧, ⑨ of Fig. 7) on the lines of one
line before and after the present line of the code frame
are subjected to the flashing control. Thus, no defi-
10 ciencies due to fringing will occur at a time of
flashing. That is, if the fringing were done when the
flashing were off, "A" would be excluded from the image
of Fig. 5D. This can be prevented so that such an ori-
ginal image as shown in Fig. 5B may be obtained.

15 Although an embodiment of the present invention has
been described in detail, the present invention is not
limited to the specific embodiment.

For example, in the previous embodiment, use is
made of a double scan monitor as CRT 9, but a 1H:24 KHz
20 monitor used with personal computers may be used instead
in the present invention. In this case, LP for LCD 10
should be modified to accommodate 640 pixels and FP may
be 70 Hz.

In the embodiment described previously, although
25 use is made of SRAM 7 and DRAM 8 as image memories,
other memories may be used instead.

Furthermore, the previous embodiment was described

with respect to the case where the present invention was applied to a videotex system. It is needless to say that the present invention may be applied to display control of other systems.

5 As described above, the present invention can control two types of display devices which are different in type of data to be handled and driving method with the aid of simple software and a small amount of hardware. In videotex system, widely used
10 binary type LCDs can be used in addition to CRTs or active matrix type LCDs. Code and photo frames can be distinguished from each other even if they are displayed one above the other.

Claims:

1. A display control device comprising:
first memory means;
second memory means; and
5 display control means comprising
(a) means for storing first data adapted to a
predetermined display device in said first memory means;
(b) means for reading the first data from said
first memory means on a time division basis in sync with
10 predetermined timing of display;
(c) means for converting the first data read out of
said first memory means to second data adapted to a
display device different from said predetermined display
device;
15 (d) means for storing the second data in said
second memory means; and
(e) means for reading the data stored in said
second memory means out of said second memory in
accordance with timing of display which is different
20 from the predetermined timing of display.
2. A display control device according to claim 1,
wherein said first memory means comprises a static
random access memory.
3. A display control device according to claim 1,
25 wherein said second memory means comprises a dynamic
random access memory.
4. A display control device according to claim 1,

wherein the first data is adapted to a cathode ray tube.

5. A display control device according to claim 1,
wherein the second data is adapted to a binary type
liquid crystal display device.

5 6. A display control device according to claim 1,
further comprising CPU means for controlling writing
into or reading from said first and second memory means
via said display control means.

10 7. A display control device according to claim 1,
wherein said display control means further comprises
timing generating means for generating predetermined
timing signals for said display control means.

15 8. A display control device according to claim 1,
wherein said display control means further comprises
address generating means for generating predetermined
addresses for said display control means.

20 9. A display control device according to claim 1,
wherein said display control means further comprises
access control means for controlling predetermined
access to said first memory means.

10. A display control device according to claim 6,
wherein said display control means further comprises
weight control means for controlling predetermined
weights to said CPU means.

25 11. A display control device according to claim 1,
wherein said display control means further comprises
erase means for controlling predetermined hardware

erasing of said first memory means.

12. A display control device according to claim 1,
wherein said display control means further comprises
decoder means for decoding the first data read from said
5 first memory means to provide predetermined R, G and B
signals.

13. A display control device according to claim 1,
wherein the first data has a plurality of frames.

14. A display control device according to
10 claim 13, wherein said converting means comprises means
for converting the first data so that said plurality of
frames can be distinguished for the second data.

15. A display control device comprising:
a first image memory for storing image data for a
15 first display device;
a second image memory for storing image data for a
second display device which is different from said first
display device in driving method and/or type of image
data to be handled;

20 first data converting means for converting incoming
image data to image data to be stored in said first
image memory;

data writing means for writing image data converted
by said first data converting means into said first
25 memory means;

first data readout means for reading the image
data, which has been written into said first memory

means by said first data writing means, on a time division basis in sync with the timing of display of said first display device;

second data converting means for converting the
5 image data read out of said first memory means to image data to be stored in said second memory means in sync with the timing of data readout of said first data readout means;

second data writing means for writing the image
10 data converted by said data converting means into said second image memory in accordance with readout addresses of said first data readout means; and

second data readout means for reading the image
data written into said second image memory by said
15 second data writing means out of said second image memory in accordance with the timing of display of said second display device.

16. A display control device according to
claim 15, wherein said first image memory is adapted
20 to store first and second brightness data corresponding to a display screen of said first display device as the image data for said first display device; and wherein said second data converting means comprises data holding means for holding the first brightness
25 data in a present display position and surrounding display positions adjacent to the present display position and the second brightness data in the present

display position, the first and second brightness data being read out by said first data readout means;

brightness deciding means for deciding whether or not the first brightness data in the surrounding display positions adjacent to the present display position held
5 in said data holding means;

brightness data mask means for masking the second brightness data in the present display position when said brightness deciding means decides the first
10 brightness data to have brightness; and

data combining means for a masked output of said brightness data mask means and the first brightness data in the present display position held in said data holding means.

15 17. A display control device according to claim 16, wherein said first image memory is adapted to store flashing data of the first and second brightness data; wherein said first data readout means is adapted to read the flashing data of the first and second
20 brightness data in correspondence with the readout of the first brightness data in the present display position and the surrounding display positions adjacent to the present display position and the second brightness data in the present display position; and wherein said
25 data holding means comprises flashing data holding means for holding the flashing data read out by said first data readout means; flashing state deciding means for

flashing states of the first and second brightness data
synchronized with the timing of display on the basis of
the flashing data held in said flashing data holding
means; and flashing mask means for masking corresponding
5 first and second brightness data when said flashing
state deciding means decides the flashing to be off.

18. A display control device comprising:

an image memory for storing first and second
brightness data corresponding to the display screen of a
10 display device;

data holding means for reading the first brightness
data in the present display position and surrounding
positions adjacent to the present position and the
second brightness data in the present display position
15 from said image memory on a time division basis and
holding them;

brightness deciding means for deciding whether or
not the first brightness data in the surrounding posi-
tions adjacent to the present position held in said data
20 holding means has brightness;

brightness data mask means for masking the second
data in the present position when said brightness
deciding means decides the first brightness data to have
brightness; and

25 data combining means for combining the mask output
of said brightness mask means and the first brightness
data in the present position held in said data holding

means.

19. A display control device according to claim 18, wherein said image memory is adapted to store flashing data of the first and second brightness data; and wherein said data holding means comprises flashing data holding means for reading the flashing data of the first and second brightness data in correspondence to the readout of the first brightness data in the present display position and the surrounding display positions adjacent to the present display position and holding them; flashing state deciding means for flashing states of the first and second brightness data synchronized with the timing of display on the basis of the flashing data held in said flashing data holding means; and flashing mask means for masking corresponding first and second brightness data when said flashing state deciding means decides the flashing state to be off.

20. A display control apparatus for image display system, substantially as hereinbefore described with reference to the accompanying drawings.